PHased Array Signal Emitter (PHASE) IC - UnPhased's 18725 Final Project

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***Abstract*—This is the final project report for team UnPhased with our PHASE IC: a six channel sine wave direct digital synthesizer for phased array applications.**

I. Introduction

The PHASE IC is a direct digital synthesizer (DDS) designed to generate the precise relative phase signals used to control a phased array. Typical phased array drivers target low resonant frequency ultrasonic transducers using digital PWM pulses with what are effectively long shift registers. On the other end of the spectrum, there are high frequency, high accuracy single output direct digital synthesizers for medical or precision equipment. Our chip, with direction guided by potential application in Dr. Gary Fedder's MEMs lab's research with a novel, micro ultrasonic transducer, aims to be a sort of middle ground: a chip with multiple, MHz-capable analog outputs to simplify driving an array of higher-end transducers or other devices.

II. Prior Work

Previously, the first prototype of the phased array driver electronics for the transducer consisted of 2 PCB boards, one digital board for generating the square wave, and one analog board providing high voltage outputs. [1] Our design combines the functionality of the two large-size PCBs with the only addition of connecting sets of op-amps to amplify our output signals so that they are capable of driving piezoelectric transducers for stimulating tactile sensations. This will contribute to the goal of making a truly wearable ultrasonic phased array for simulating tactile sensation.

III. System Architecture

A. Overview

Our chip consists of 6 independent DDS channels, each with its own numerically controlled oscillator (NCO) and 8-bit current steering DAC. Programming the DDS channels is

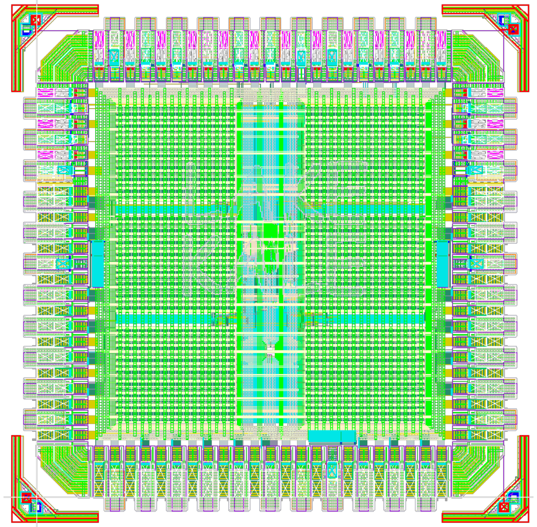


Fig. 1. Layout view of completed chip

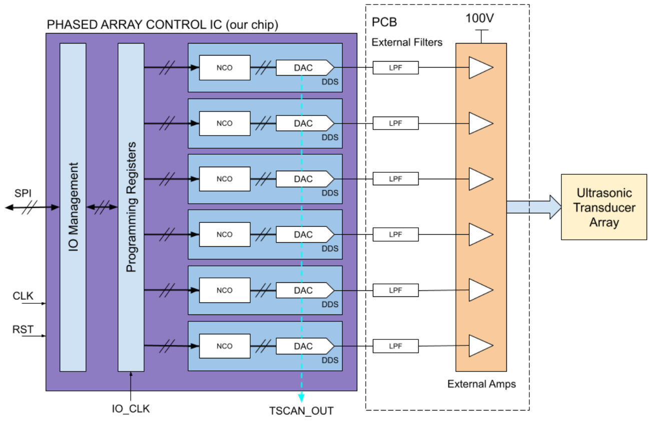


Fig. 2. System Overview

done through a standard SPI interface. All control inputs are buffered until the user commits them to the digital synthesizers using a separate input, allowing for synchronous phase, frequency, and amplitude changes across all output channels. A global system clock determines the effective base frequency for all output channels and operates independently of the SPI interface. The chip is designed to be capable of generating up to a 20 MHz sine wave (with a 320 MHz input system CLK) with 16 distinct phase offsets and 4 bit amplitude control per channel. With 24-bit frequency resolution, each output has a 5 Hz frequency resolution with a 320 MHz system clock.

The chip can be used as originally conceived to drive multiple transducers in a phased array at the same frequency and with varying relative phase offsets and amplitude modulation. However, due to the fact that each channel is independently frequency programmable, it can also be used to generate multiple sinusoidal signals at different frequencies for other applications.

B. Digital

There are three main digital components: the SPI peripheral and IO management modules, the programming registers, and the six Numerically Controlled Oscillators. Figure 3 shows the architecture of these digital components.

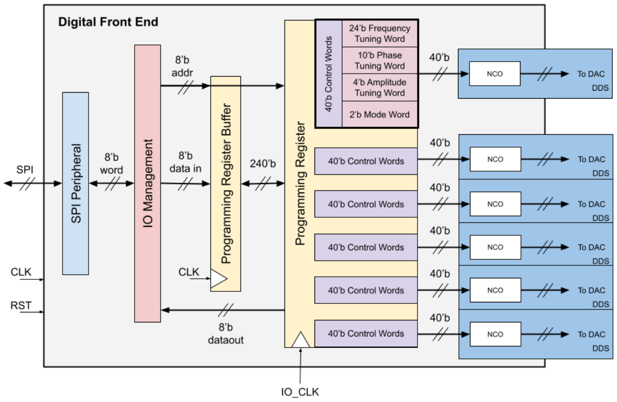


Fig. 3. Digital System Overview

1) SPI and I/O Handler: The SPI peripheral operates in standard full-duplex mode 0 (CPOL=0, CPHA=0), capable of reading in 8 bits of data and outputting 8 bits of data per transaction on the falling and rising edges of the SPI clock, respectively.

The IO management module serves as the bridge connecting the SPI peripheral to the rest of the chip. As the programming registers are 40 bits wide, with each internal turning word a different width, the IO management module is responsible for parsing the variable number of input bytes per communication into the intended address and data.

For each communication, the first byte from the SPI peripheral is the instruction byte, which contains information about which channel to write to, which parameter to modify, and whether to write or read. This sets the state of the IO management module, which then reads in the next variable number of bytes as data to be written to target programming register. The instruction will determine which channel's 24-bit Frequency Tuning Word(FTW), 10-bit Phase Tuning Word(PTW), 4-bit Amplitude Tuning Word(ATW), or 2-bit Mode configuration the following data bytes intend to write to. Table I details the instruction byte format.

TABLE I
INSTRUCTION BYTE FORMAT

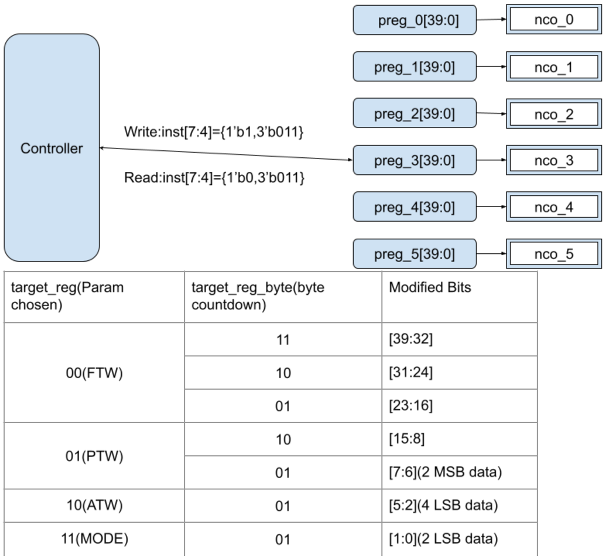
Bit	Use
7	1 for Write, 0 for Read
6:4	Target Channel
3	*unused*
2:1	00: FTW 01: PTW 10: ATW 11: MODE
0	1 for Valid communication

2) Programming Registers: The programming registers are 40 bits wide for each channel (240'b in total for 6 channels) and contain the value for the Frequency Tuning Word (FTW), Phase Tuning Word (PTW), Amplitude Tuning Word (ATW), and MODE setting used to set the output behavior of the channel's NCO.

The IO management module writes to an identically sized buffer of the programming registers. This buffer holds all of the intended changes to the programming registers, thus preventing unsynced, incremental updates from happening upon each completed SPI transaction. The controller can commit the input data via the IO_CLK input, copying the buffer contents to the actual programming registers, which then update the behavior of the NCOs. Upon a system reset, the programming registers are initialized to a zero state, but the buffer is instead reset to a pre-determined *non-zero* state, allowing for a quick IO_CLK toggle after a reset to immediately generate a sinewave signal at each output. The values of the programming registers can also be read back to the controller via the SPI peripheral. This reads the current state of the programming registers, not the buffer, allowing the controller to verify the current state of each of the DDS channels.

Figure 4 demonstrates the internal IO management to programming register logic.

3) Numerically Controlled Oscillator: The Numerically Controlled Oscillator (NCO) is responsible for turning the programmed control words into the output of the digital section: the 8-bit value to set the output voltage of its corresponding DAC. It consists of a phase accumulator (PA), a phase-to-amplitude converter (PAC), and a multiplier. The phase accumulator is a 24-bit feed-back adder that increments by the value of the Frequency Tuning Word (FTW) at each clock cycle. Figure 5 shows the structure of the phase accumulator. This accumulated phase is offset by the Phase Tuning Word (PTW) and then the 10 MSB are used to index into a sine wave value look-up table in the PAC. This means the lower 14 bits of the phase accumulator are used to interpolate between the values in the sine wave look-up table, and the top 10 bits determine how much to increment the look-up table index.



target_reg(Param chosen)	target_reg_byte(byte countdown)	Modified Bits
00(FTW)	11	[39:32]
	10	[31:24]
	01	[23:16]
01(PTW)	10	[15:8]
	01	[7:6](2 MSB data)
10(ATW)	01	[5:2](4 LSB data)
11(MODE)	01	[1:0](2 LSB data)

Fig. 4. Programming Register and IO Management Diagram

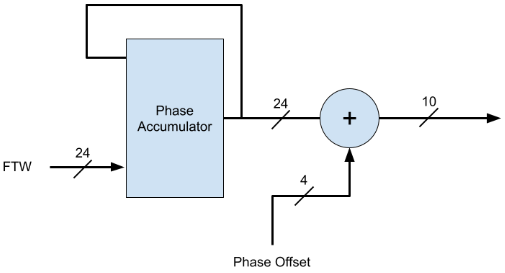


Fig. 5. Phase Accumulator Diagram

The Phase-to-Amplitude Converter (PAC) is responsible for converting the phase output from the NCO into an amplitude-representing 8 bit value. This is simply implemented as a 8-bit, 256 entry sine wave look-up table (”Sine ROM”), with the 10 MSB of the phase accumulator as the index. The additional 2 bits of the input address width versus the output value width improve the spurious-free Dynamic Range (SFDR) of the NCO. Quarter processing was used as a compression method; only the values of one quarter of a sine wave are stored in the PAC, and the other three quarters are generated by mirroring the stored values. The 2 MSB of the phase was used to determine the quadrant of the sine wave.

Before being transmitted to the thermometer encoder, the signal amplitude is adjusted based on the 4-bit ATW. The relationship between the original output from NCO and the adjusted output can be described with the following equation:

$$NCO_{adjusted} = NCO_{original} * (ATW + 1) >> 4 \qquad (1)$$

This means that when the ATW is zero, the output waveform oscillates between 0-60mV, and the maximum amplitude, 1Vpp, is reached only when ATW=15(4’b1111). Figure 6 shows the structure of the PAC and Multiplier.

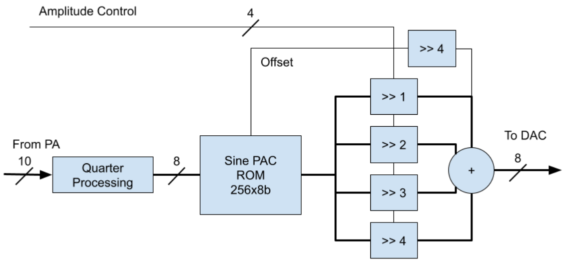


Fig. 6. Phase-to-Amplitude Converter and Amplitude Modulation

4) Reset: An important part of debugging any chip is the ability to set it to a known state. Each digital module utilizes an asynchronous reset, ensuring that regardless of the current clock behavior, the registers will be set to their default value. In order to prevent potential metastability associated with coming back from a reset asynchronously, a simple 2 flip-flop reset synchronizer was added, which causes the *rising* edge of the reset distributed to the registers in the chip to be synchronous, while maintaining an asynchronous reset assertion.

C. Analog

The analog design of the DDS consists of 6 8-bit current-steering unary digital to analog converters (DACs). The DACs are a unary design, meaning that they are made up of an array of identical unit cells, in order to reduce nonlinearity across the full digital control range. The DACs are current-steering to mitigate mismatch errors associated with resistor-based DACs and for the benefit of higher speed.

1) Unit Cell: Each DAC is comprised of 256 identical unit cells arranged in an array. 255 of them are actual functioning cells that contribute to the output and 1 dummy cell is for probing crucial nodes of the design. The unit cells are controlled with a 4 to 15 row and column thermometer decoder, so that the four most significant bits of the digital word correspond to the row selection, and the four least significant bits correspond to the column selection (Fig. 7).

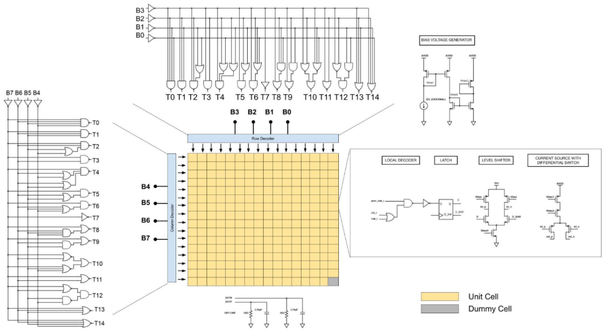


Fig. 7. DAC Architecture

Each unit cell consists of a local decoder, a level shifter, and a current steering circuit (Fig. 8). The local decoder determines the state of the unit cell depending on the row and column indices. The level shifter shifts the digital logic voltage to an analog voltage input for the current steering circuit. The level shifter is tuned to minimize glitch energy during the current steering transitions. The current steering circuit steers a unit of current toward one of two loads on the differential output of the DAC. The difference in voltage seen over these loads is then proportional to the digital word input. A cascode current source is used in the circuit for a better matching output current and larger output resistance.

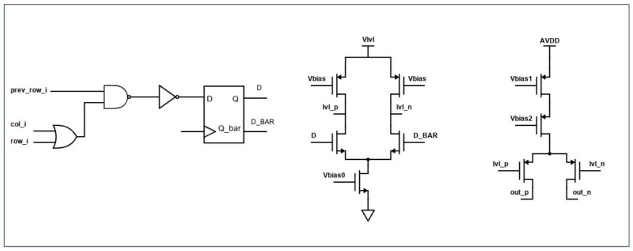


Fig. 8. Unit Cell Architecture

2) Bias Voltage Generation: The bias voltage generation is executed with an external pin to an ideal current source, and a series of current mirrors tuned in size and DC current to generate the voltage bias needed in the unit cell (Figure 9). The current mirror here pulls the same amount of current as the differential current steering circuit. This design allows us to tune the output current over the DAC loads with a feedback loop probing the current output of a unit cell dummy cell, and controlling the ideal current source input.

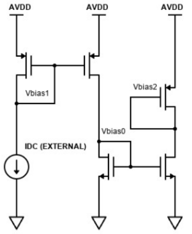


Fig. 9. Bias Voltage Generation

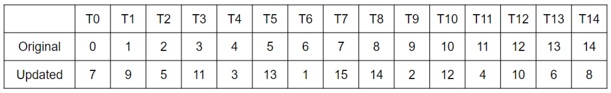
The bias voltage generation will require feedback control on the PCB to compensate for operating power and temperature variation. Critical nodes of the analog design are probed with external pins in a dummy unit cell for debugging and compensation purposes. These probe points are the DC current output of the dummy cell, the drain voltage of the current source, and the output voltage of the level shifter.

The dummy cell output current is measured off-chip and used to control the ideal current source input to the reference generation circuitry. This ensures a constant current output from each current cell over all operating conditions.

The drain voltage of the current source is probed to ensure that the current source of the current steering circuitry operates in saturation (and thus pulls the designed DC current). The drain voltage of the current source can be controlled with the level shifting voltage supply, which is the HIGH voltage for the switching transitions in the current steering structure. If the drain voltage of the current source is too high, the level shifting voltage supply must be lowered.

The level shifting output is probed in the dummy cell as well so as to control the LOW level shifting value which inputs to the differential pair. The LOW level shifting value is determined by the voltage drop over the active load in the level shift (which is biased by an externally connected bias voltage, vrbias). The level shift output voltage is tuned to shift the digital logic voltage to analog voltages which bias the differential pair in the current steering circuit symmetrically. One differential transistor operates in cut-off and the other operates in triode region, and ensuring that the switching time for the differential pair is equal helps minimize glitch energy seen at the output. If the drain voltage of the current source varies, the symmetric bias point for the PMOS differential pair must be adjusted accordingly.

3) Thermometer Decoder: The thermometer decoder controls the unit cell current steering with the digital 8-bit input. The glitch energy in the analog output of the DAC is a product of transient states in the unit cells as they turn on/off. In order to minimize glitch energy, we designed the thermometer decoder outputs to retain the state of as many unit cells as possible during digital control word transitions. The thermometer decoder output mapping to the row/column indices provides an optimum turn-on sequence for row/column combinations (Figure 10, [Wang, D]). For debug purposes, the thermometer decoder is connected to its own scan chain output.



	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14
Original	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Updated	7	9	5	11	3	13	1	15	14	2	12	4	10	6	8

Fig. 10. Thermometer Decoder Output Mapping

D. DAC Specifications

The DAC is designed to operate at 320 MSPS, which allows for a 20MHz output signal with 16 phase shifts. The resolution is 8 bits and the output voltage when connected to a 50 ohms load is 1V which means the least significant bit has a voltage of 3.9mV. The power demands of the DAC are predominantly from the level shifter and the current steering circuit (Table 2). The level shifter power input is a separate voltage reference supplied through an external pin. The current steering circuit is supplied through AVDD.

IV. Implementation

Our chip was constructed with the Digital on Top (DoT) methodology in Cadence Innovus. Minor DRC corrections and chip finishing (adding dummy and seal ring) were done in

TABLE II
DAC Power Specifications

Specification	Level Shifter	Current Steering
DC Current/Cell	8.5uA	78.125uA
Voltage Supply	800mV	1.8V
Total Power	10.4mW	216mW

Cadence Virtuoso. The final chip layout is shown in Figure 11, and Table 3 provides a comparison of our chip and a current DDS product.

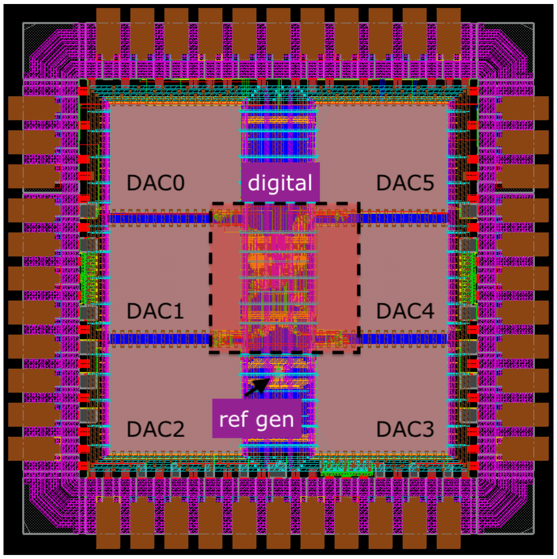


Fig. 11. Innovus Full Chip

TABLE III
Chip Stats

	Our Design	AD9854 [3]
Technology	TSMC 28nm HPC+	0.35um CMOS
Die Area	1mm^2	196mm^2
Core Area	0.43mm^2	90.25mm^2
Frequency	320MHz	300MHz
Core Supply Voltage	0.9V	3.3V
Analog Supply Voltage	1.8V	3.3V
Max Power Consumption	278mW	4.19W
DAC Resolution	8-bit	12-bit
Frequency Resolution	24-bit	28-bit
Phase Resolution	10-bit	14-bit
Amplitude Resolution	4-bit	12-bit
Num. Output Channels	6	2

A. *Floorplanning*

1) Placement: The primary consideration during floorplan were the DACs. They are spread apart as much as possible in the core area. The DACs are large macros, big enough to nearly completely cover the one dimension of the core in a stack of three. As we had six DACs and realistically only one layout, we had to make sure that the DACs' IO was set in such a way to allow efficient connections to the output IO cells on the edge of the chip, internal core connections, as well as supply and bias voltage connections. The orientations of the DACs are mirrored down the center y-axis, which allows for three things. First, the output ports are at one corner of the DAC layout. The mirrored layouts allow these ports to align at the edge of the core area towards their respective IO cells. Second, perfectly mirrored orientations allowed for block-to-block power connections. The DAC layout spans all 9 standard metal layers, making it impossible for top-level routing to go over a DAC. However, it spans all metal layers as it implemented extensive internal grids for distribution of power and analog voltage biases. We were able to connect these internal grids at the top level with block *pin to pin* connections, facilitated by the fact that all the DACs were perfectly aligned and oriented relative to each other.

Lastly, with the DACs situated, the remaining usable core area was an approximately 150 um wide vertical strip down the center and thin horizontal stripes running between DACs. The most sensible place for the digital components was thus directly in the center. The DACs were designed to have the digital control and debug signal ports along the top edge, close to the upper-left corner. With the mirrored DAC orientations, all these ports would be as close as possible to the digital core. You can see were these ports are on the DAC (and thus their relative orientations to each other) by observing where there are clusters of digital cells and top-level routing (red and yellow) along the DACs in figure 11.

The bias reference generator for the DACs was also placed in the center vertical stripe, but closer to the bottom edge of the core area. The reason for this is two fold. First, moving it out of the direct center of the core prevent it from interfering with the digital placement and routing. Second, its essential connections are at the bottom edge of the die.

2) IO: The peripheral IO cells were mostly determined by two simple rules, one required and one arbitrary: First, Digital and Analog IO cells must be together in their own domains. Second, the DAC outputs should be as close as possible to their respective IO cells.

The first rule resulted in the digital IO being grouped together on the top edge (and upper parts of the left and right edges), with the analog IO cell domain taking the rest of the ring. The second rule meant the DAC outputs were to be on the left and right sides of the die (as their orientations had already been fixed by reasons described in section IV-A1, leaving the bottom edge for analog bias inputs and debugging measurements.

B. *Power Planning*

The power distribution of the chip is somewhat unconventional due to the layout of the DACs, as previously mentioned in section IV-A1. The primary connections across the core area itself is made by connections in the upper metal layers (M8 and M9) between the DACs themselves. The DACs have built in power distribution grids at these top layers, and by exposing the ends of these internal grid stripes for AVDD, VDD, and VSS, we were able to connect them to each other using block pin-to-pin special routes. The DAC power grids are also connected to a thick 5um core ring running around the core area for each power net, through which the power IO cells are connected to the internal core. The resulting power distribution is shown in figure 12, where the internal DAC grids and top-level added connections are clearly visible.

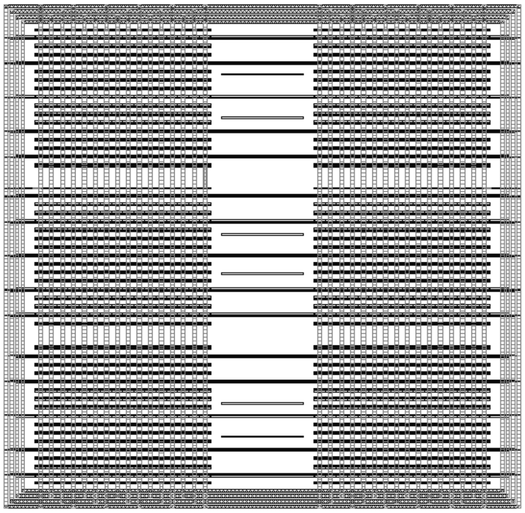


Fig. 12. Chip AVDD, VDD, VSS grid on Metal 8 and Metal 9

The bias voltage distribution also required special attention at the top level, as variations caused by IR drop could negatively affect the performance of the DACs. To that end, a second set of power grids was implemented in the DACs, this time for the bias voltages, in the M6 and M7 layers. To prevent special route congestion, despite being on separate metal layers, the bias voltage rings were offset from the primary supply rings, and did *not* have core rings. Instead, block rings were formed around the left and right set of 3 DACs, and connected to each other via power stripes across the center of the core area. Similar to the supply voltages, the DACs also had internal bias voltage grids. Multiple pins to these bias voltages grids were exposed for a more robust connection to the surrounding bias rings.

The reference generator acted like a routing hub, with its block rings connecting the DAC bias rings as well as the supply block rings and vertical center stripes.

For digital core power, special care was taken to make sure the supply routing from the top M9 level could punch down all the way to M1 to tap the VDD and VSS rows, especially in the thin horizontal areas between DACs. No horizontal power routes under M9 were allowed between the DACs, and the block rings for the supply voltages were set to M5 in the center core area. Additional vertical center power stripes were added down the center to ensure that the digital core had ample supply connections.

In addition to the transmission gates discussed later in IV-D2, there were two supply ESD prevention techniques used for our chip. The first was the insertion of additional, unbonded VSS IO cells in-between the IO cells, as recommended by the TSMC 28nm IO cell design guide. The second was the addition of ESD clamps on the AVDD IO cells, which stand between the AVDD from the IO cell and the internal AVDD power routing.

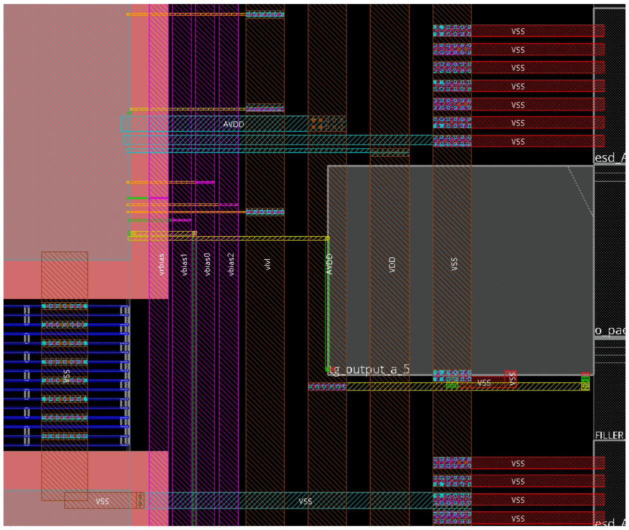


Fig. 13. Special Routing close-up

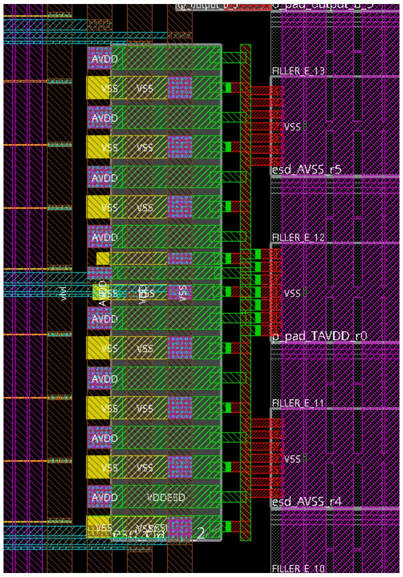


Fig. 14. AVDD ESD Clamp

C. Analog Layout

1) Layout techniques: Analog layout has two components on the block level which are the DACs and the reference voltage generation circuit. Techniques such as common centroid layout and the placement of dummy transistors surrounding the active functioning transistors are consistently applied through analog layout design to improve the matching of devices such as the current source and make the design more resilient to process variations.

2) DAC: Inside the DAC, there are two sub-blocks which are the the unit cells and the thermometer decoder. 256 unit cells are arranged to form a 16 by 16 array including the dummy cell placed at the bottom corner of the array (Figure 15). To increase the accessibility to the supply voltage and bias voltages, the DAC layout design contains local grids for signals. The bias voltage grid is built by the lower metal layer while the supply voltage (AVDD and DVDD) and ground are built on the upper metal layer with thicker traces to accommodate the high current going through them. They will be connected in between the DACs on the chip level to form a larger scale of power grids and power rail rings surrounding each DAC and the whole chip. In addition, since each current cell making up the DAC (Figure 16) contains a local decoder made with standard digital cells, a clock grid is constructed to reduce the latency.

The row and column thermometer decoders are made of the logic gates from the standard cell library and they are arranged to be placed on the upper corner of the DAC layout) (Figure 17). Their outputs are also built to a grid throughout the layout design of the DAC so as to reduce the delay of digital control words to each unit cell. The standard cells used to build the local decoder and the thermometer decoder are carefully picked for a balance of both layout area and performance.

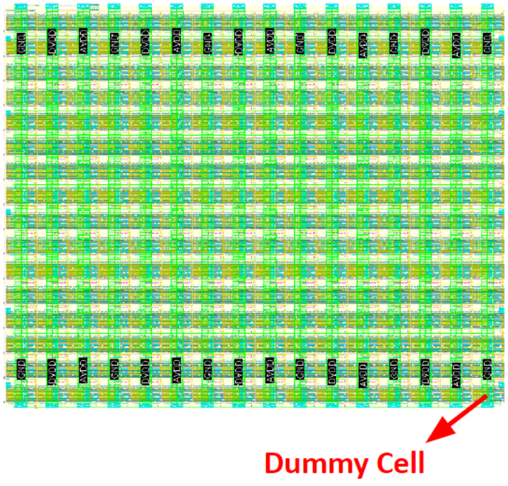


Fig. 15. DAC Layout

3) Bias Voltage Generation: The bias voltage generation circuit layout was executed with the same common-centroid techniques as the DAC (Figure 18).

D. Integration

1) Scan Chains: There are two independent scan chains in the design: one for the entire digital front end, and another for all the DACs' thermometer decoder outputs. The digital front end scan chain shares the SPI interface's input and output, but uses the system CLK as the scan clock (as this clock is already distributed to all the relevant registers). The thermometer decoder scan chain is meant simply as an independent scan-out path for debugging the behavior of the decoders (the input to the chain is not important, as the registers part of the scan chain are not actually in the datapath for the DACs). It was added on the *digital* side during top-level integration, connecting to prepared, combinations only decoder outputs from the DACs. The timing between the source register (NCO output) and decoder capture register is not important, the registers only exist for the debug scan and in the debug scenario, the digital front end will be held static. By keeping these two chain separate, we can operate the digital front end normally while checking the DACs' decoder outputs, without needing to scan in and out the whole chip's register states.

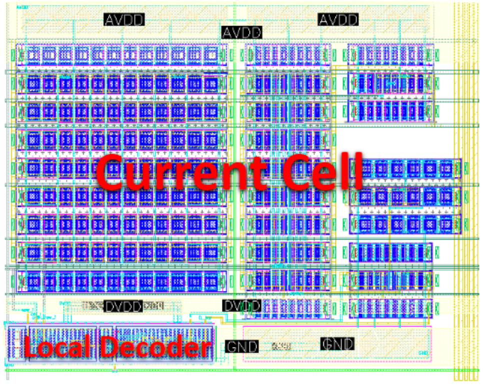


Fig. 16. DAC Layout

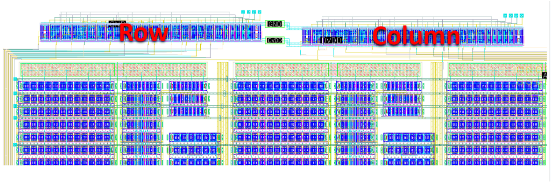


Fig. 17. Thermometer Decoder

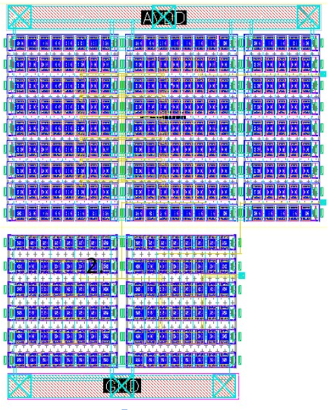


Fig. 18. Bias Generation

2) Transmission Gate: The transmission gate was a last-minute, critical addition to the analog design. The DACs were originally directly connected to the IO cells through the distribution grids and rings. However, this led to numerous Latch-Up and ESD DRC violations since the transistors in the DAC were not properly surrounded by guard rings.

To combat this, the transmission gates were added as a properly guarded buffer between the DACs and the IO cells. It functions as a bilateral switch between the analog IO ring and the core (Figure 19). Based on the guidelines for ESD placement, the drain terminals of the transistors are connected to the IO pads, and the source terminals are connected to the core analog devices. In order to prevent significant voltage drop, the transistors used in the transmission gates were designed to have a large channel width and minimum channel length (Figure 20). For the nets that would be pulling or sinking a lot of current such as the DAC outputs and the voltage HIGH of the level shifter, two transmission gates are connected in parallel to further reduce the voltage drop.

These transmission gates were inserted automatically in the digital construction flow and connected to the IO cells by abutment, and routed to the target internal net with Innovus Special (Power) Routing.

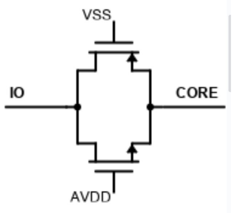


Fig. 19. Transmission Gate Architecture

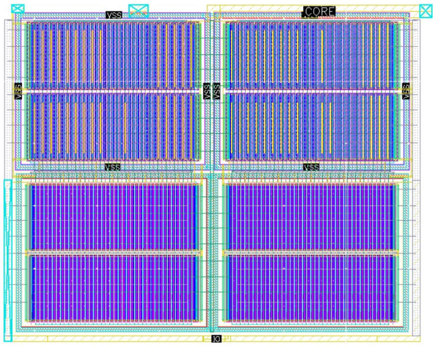


Fig. 20. Parallel Connected Transmission Gate Layout

V. Simulation Results

A. DAC Performance

1) Temperature and Supply Voltage Corners: The DAC performance was tested over 5% supply voltage variation and at 27°C and 100°C. At nominal condition (AVDD=1.8V, 27°C) the DAC is able to output the maximum of 1V differential output, and the glitch energy is largely mitigated by the switching sequence of the thermometer decoder applied in the design. Fig. 21 shows the single-end output of the DAC for all temperatures and supply voltage corners and the clock frequency is set to 320MHz.

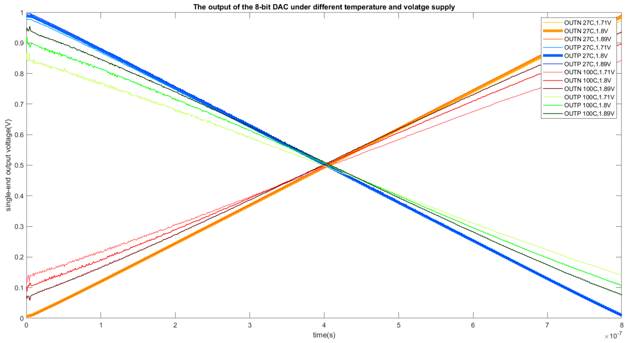


Fig. 21. DAC Single-Ended Output

2) Nonlinearity: DNL of DAC plotted over 5% power rail variation and at 27°C and 100°C. The DNL is well under 0.5 LSB at nominal conditions (Figure 22). We see significant DNL at non-nominal temperature and power rail conditions. This tells us that the bias generation circuit will need to be controlled on the PCB with a feedback loop.

The INL of DAC plotted was also analyzed over 5% power rail variation and at 27°C and 100°C (Figure). INL at nominal conditions is under 2.5LSB (10mV error) at the extremes of the digital word input (Figure 23). We again see significant INL at non-nominal temperature and power rail conditions. This tells us that the bias generation circuit will need feedback control on the PCB level.

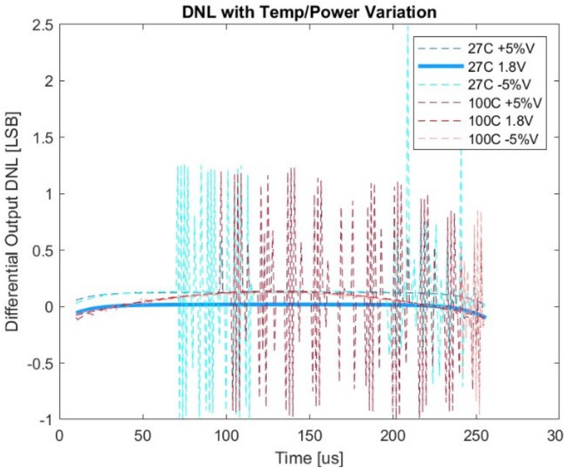


Fig. 22. DNL

B. Digital

Digital simulations were run on the front end digital components with Cadence Xcelium to ensure intended functionality at RTL and synthesized levels of construction. In Fig. 24 and

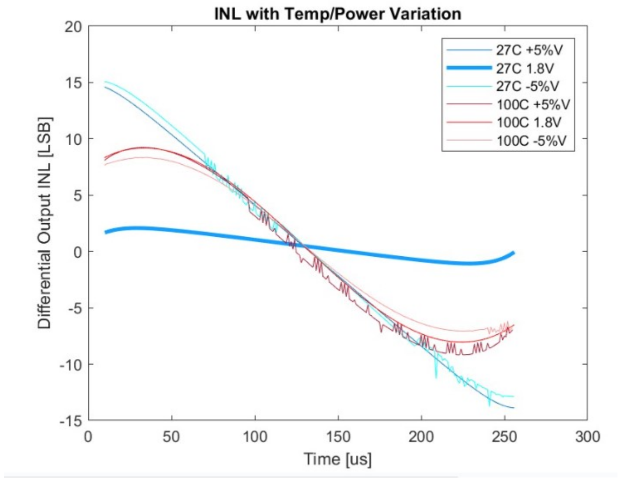


Fig. 23. INL

25, by updating FTW and PTW, the change in period and current phase of the sine wave could be observed. We relied on top-level AMS simulation in ADE to ensure the functionality of the digital components post-layout.

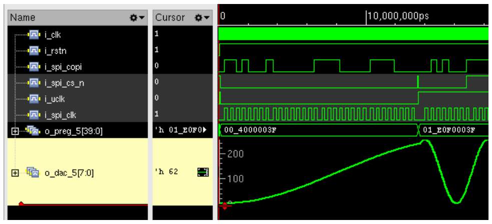


Fig. 24. Xcelium Simulation demonstrating an output frequency change

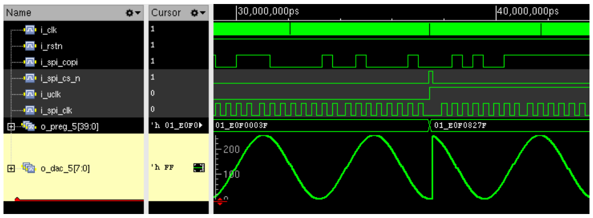


Fig. 25. Xcelium Simulation demonstrating an output phase change

C. Full Chip

To ensure that the digital and analog parts of the system would work coherently together, we attempted to run the complete chip-level simulation in ADE with the Spectre simulator. The top-level signal inputs (all digital) were generated by a stripped-down test bench and saved as a VCD file. This VCD was then imported as the input vector file for the Spectre simulator. In figure 26, we have around 3 μs of full chip running with a 320 MHz clock simulated, with the first 2 μs used for programming the mode (a single SPI transaction) to one of the DDS channels. After around 2 μs, after the user IO_CLK has gone high and committed the new settings to the programming registers, we can see that the differential output has started outputting a small, 60mV sine wave, which is the default minimum amplitude.

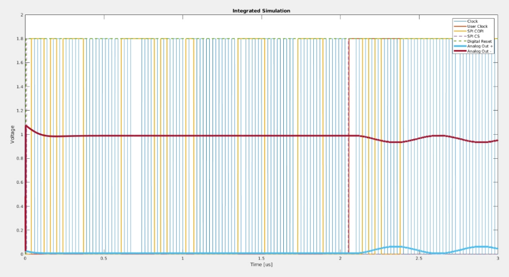


Fig. 26. Integrated Simulation

It was also through a full chip simulation that we discovered that our original transmission gate solution to the ESD and latch-up DRC errors was functionally problematic (too high of a resistance that severely affected any input or output that drew non-trivial current), and prompted a last minute redesign.

TABLE IV
AREA AND POWER SPECIFICATIONS

	Component	Qty	Area (ea.)	Power
Analog	Entire Analog	1	0.32mm^2	278mW
	Level Shifter	1		10.4mW
	Current Steering	1		216mW
	DAC	6	0.053mm^2	36mW
Digital	Entire Digital	1	0.012mm^2	0.9uW
	NCO	6	0.0012mm^2	0.13uW
	IO Management/Scan	1	0.0014mm^2	
Total			0.33mm^2	278mW

VI. Individual Contributions

A. Ellie

Analog schematic design, characterization, layout, AMS integration

I was responsible for working with Kaiyuan on the DAC design and simulation on the schematic level, as well as characterizing its performance and optimizing for linearity, glitch energy, and area. Also responsible for high-level integration of the analog and digital designs in order to fulfill all requirements for AMS tape-out.

B. Kaiyuan

Analog schematic design, characterization, layout, and top-level layout integration

I worked with Ellie on the analog block design, simulation, and DAC performance characterization. I was also responsible for the complete DAC layout design and the integration of analog and digital layouts at the chip level such as designing blockage of analog block placement and manually fixing DRC and LVS violations after integration.

C. Alan

Digital design, testing, and full chip simulation

Primarily responsible for the design of the digital front end, formulation of the testing plans, as well as implementation of the front end. Ran through the Innovus Foundation Flow up to post-signoff gate-level netlist. I also set up the Spectre mixed-signal simulation to validate the functionality of the full chip.

D. Leon

Digital design, layout, and top-level integration

I created the design for the entire digital front end of the chip, including the SPI peripheral, IO management, and NCO, and implemented all but the NCO. Digital-side construction, and thus top-level construction, was also managed by me, including netlisting, chip floorplan, power planning, and top-level analog macro integration.

Class Feedback

- The instructor-led project check-ins were very helpful and a good motivator to make continuous progress.
- Sometimes important information, such as design review presentation schedule, was inconveniently posted at the last minute.
- Not really a fault of the class, as the class is called ”Advanced Digital Integrated Circuits”, but there was much more support from the TAs / instructors for digital / Innovus related issues than for analog ones. Not sure how it could be done but someone with cross-domain tapeout experience would make analog and AMS designs more approachable.
- Quirks about the ECE machines, tools, etc. of the semester should be conglomerated somewhere as a master reference. (Things like: LVS run directory must be in scratch or Andrew space instead of an ECE directory).
- An exact list of the DRCs that are waivable by Muse, *from Muse* themselves could be helpful for teams that aren't doing standard digital flow and who may encounter less common DRCs.
- Hope that there could be more specific assignments related to the Back-End implementation of the chip. While it's true that topics like floorplanning/power distributions are covered in lectures, some still had trouble understanding functionality and reasoning behind Back-End scripts.

References

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[2] Wang, D.; Guo, X.; Zhou, L.; Wu, D.; Luan, J.; Liu, H.; Wu, J.; Liu, X. A 3GS/s 12-bit Current-Steering Digital-to-Analog Converter (DAC) in 55 nm CMOS Technology. *Electronics* **2019**, *8*, 464. https://doi.org/10.3390/electronics8040464

[3] Analog Devices, ”AD9854: CMOS 300 MSPS Quadrature Complete DDS Data Sheet (Rev.F)” Oct 31, 1999.